



# Intel<sup>®</sup> I/O Controller Hub 6 (ICH6) Family

White Paper

---

*October 2004*



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® I/O Controller Hub 6 (ICH6) / Intel® I/O Controller Hub 6R (ICH6R) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

I<sup>2</sup>C is a two-wire communications bus/protocol developed by Philips. SMBus is a subset of the I<sup>2</sup>C bus/protocol and was developed by Intel. Implementations of the I<sup>2</sup>C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel, Intel Centrino, and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2004, Intel Corporation



# Contents

---

1	Overview .....	5
2	Highlights .....	7
2.1	Direct Media Interface (DMI) .....	7
2.2	PCI Express* .....	7
2.3	Intel® High Definition Audio (Intel® HD Audio).....	8
2.4	Serial ATA (SATA).....	9
2.5	SATA with the Advanced Host Controller Interface (AHCI) .....	9
2.6	SATA with Intel® Matrix Storage Technology.....	10
3	Additional Features .....	11
3.1	High-Speed USB 2.0 .....	11
3.2	Alert Standard Format (ASF) Management Controller.....	11
3.3	AC '97 2.3 Controller .....	12
3.4	LAN Controller .....	12
3.5	PCI Interface.....	12
3.6	System Management Bus (SMBus 2.0) .....	12
3.7	IDE Interface.....	12
Appendix A	.....	14

## Revision History

---

Revision Number	Description	Revision Date
-001	<ul style="list-style-type: none"><li>Initial Public Release.</li></ul>	June 2004
-002	<ul style="list-style-type: none"><li>Removed references to Intel® Wireless Connect Technology</li></ul>	October 2004

# 1 Overview

---

The Intel® ICH6 family, for desktop systems, consists of the Intel® ICH6 and Intel® ICH6R I/O controller hubs and is an integral part of Intel chipsets in conjunction with the (Graphics) Memory Controller Hub (G)MCH. Connected to the (G)MCH through the Direct Media Interface (DMI), a new chip-to-chip interface, the ICH6 provides platform features and capabilities for quality, robustness, and longevity.

ICH6 platforms enable the next generation of I/O communication via PCI Express\*, enhanced audio via the Intel® High Definition Audio interface, and improved desktop storage with integrated Serial ATA (SATA). The ICH6 also supports eight high-speed USB 2.0 ports and includes other familiar legacy features such as Integrated LAN, an ASF Management controller, AC '97, IDE, support for PCI Rev 2.3 and ACPI 2.0 compliant power management logic.



In addition to the features supported by ICH6, the ICH6R incorporates an Advanced Host Controller Interface (AHCI) enabling Native Command Queuing for a higher performance storage interface. Additionally, the Intel® Matrix Storage Technology controller has support for both RAID Level 1 and RAID Level 0. Furthermore, RAID 1 and RAID 0 can be combined, in a two-drive configuration, to form a disk array with two volumes. These enhancements allow up to 300 MB/s bandwidth on data reads and writes through data striping, and/or data redundancy through data mirroring.

§



## 2 Highlights

---

The ICH6 family has been designed to meet the needs for today's applications and the increased demands of future applications. In this section, several key ICH6 family features will be highlighted: Direct Media Interface, PCI Express\*, Intel High Definition Audio (Intel HD Audio), Serial ATA (SATA), SATA with the Advanced Host Controller Interface (AHCI), and SATA with Intel Matrix Storage Technology controller support.

### 2.1 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the next generation chip-to-chip interconnect between the ICH and the (G)MCH, designed to meet increasing bandwidth needs and usage models. DMI supports 2 GB/second concurrent transfer rates via two unidirectional lanes, eliminating the hub interface bi-directional implementation, thereby laying the foundation for less contention. Additionally, DMI integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities providing improved quality of service. This high-speed interface ensures that the I/O subsystem (PCI Express, Intel High Definition Audio, SATA, USB, etc.), receives the bandwidth necessary for peak performance.

### 2.2 PCI Express\*

PCI Express is the next generation high performance general input/output architecture. This interface is designed to handle the bandwidth required for Gigabit Ethernet, digital video capture, and other high-bandwidth usage models. The ICH6 provides 4 (x1) PCI Express ports with each port supporting up to 5 Gb/s concurrent bandwidth (2.5 Gb/s in each direction).



PCI Express is a high speed, low voltage, serial pathway for two devices to communicate with each other. PCI Express utilizes a protocol that allows devices to communicate simultaneously by implementing dual unidirectional paths between two devices. PCI Express gives more for less, providing more bandwidth with fewer pins. PCI Express is designed to leverage the strengths of yesterday's general I/O architectures while addressing architectural and mechanical issues such as bandwidth constraints, protocol limitations and high pin counts.

PCI Express adopts a split transaction protocol that is improved over that of PCI-X. PCI Express replaces the device-based arbitration process of conventional PCI and PCI-X with flow-control-based link arbitration that allows data to pass up and down the link based upon traffic class priority.

PCI Express supports advanced error reporting to provide a higher quality of service.

PCI Express has been defined to be backward compatible while adding feature enhancements. Backwards compatibility is accomplished by all PCI Express hardware elements having been defined with a PCI-compatible configuration space representation. PCI Express therefore, is defined to be 100-percent compatible with conventional PCI-compliant operating systems and

their corresponding bus enumeration and configuration software. This allows the architecture to be transparent to the operating system. A system with PCI Express architecture looks to software exactly like a conventional PCI-based system with feature enhancements.

PCI Express has been defined to support existing ATX and server form factors while supporting evolving form factors. PCI Express defines connectors that are similar to conventional PCI connectors. This allows PCI Express connectors to occupy the same space once occupied by traditional PCI connectors. PCI Express add-in cards follow the same height and length requirements that are defined for conventional PCI. Additionally PCI Express-based add-in cards use the same I/O bracket to secure cards to the chassis as conventional PCI.

## 2.3 Intel® High Definition Audio (Intel® HD Audio)

Intel High Definition Audio is an evolutionary technology that replaces AC '97. This next generation architecture for implementing audio, modem, and communications functionality was developed to enhance the overall user PC audio experience and to improve stability. Intel HD Audio facilitates exciting audio usage models while providing audio quality that can deliver Consumer Electronics levels of audio experience.

Furthermore, Intel HD Audio capabilities provide compelling communication usage models for the PC as a collaboration and communication device.

The Intel HD Audio controller supports up to three codecs. With three Serial Data In (SDI) and one Serial Data Out (SDO) signals, concurrent codec transactions on multiple codecs are made possible.

The SDO connects to all codecs and provides a bandwidth of 48 Mb/second. Each of the three SDI's are typically connected to a codec and has a bandwidth of 24 Mb/second. In addition, the controller has eight non-dedicated, multipurpose DMA engines (4 input, and 4 output). This allows potential for full utilization of DMA engines for better performance than the dedicated-function DMA engines found in AC '97. In addition, dynamic allocation of the DMA engines allows link bandwidth to be managed effectively and enables the support of simultaneous independent streams. This capability enables new exciting usage models (e.g., listening to music while playing a multi-player game on the internet).



Intel HD Audio has support for multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz. On input, the ICH6 adds support for an array of microphones that can be used for enhanced communication capabilities and improved speech recognition. The Intel HD Audio controller is Universal Audio Architecture (UAA) compatible providing native OS audio support while also supporting isochronous data transfers for glitch-free audio to the system.





## 2.4 Serial ATA (SATA)



The ICH6 enables next generation Serial ATA (SATA) drives by integrating a 4-port Serial ATA controller. The ICH6 supports up to four SATA devices, providing an interface for SATA hard disks and optical storage devices. The connection between motherboard and SATA storage device is accomplished by using a thin, flexible Serial ATA cable. Since Serial ATA connections are point-to-point, the four SATA channels can have independent timings resulting in transfers occurring with no shared bandwidth. The individual channels can support Serial ATA transfers up to 1.5 Gb/s (150 MB/s), allowing headroom for ever-increasing Hard Disk Drive (HDD) media rates. The SATA controller can be configured to the standard primary and secondary channels, or with proper software support, can be configured as a Native IDE controller.

The ICH6 SATA controller is designed provide SATA swap bay when enabled with a notification mechanism and proper BIOS and operating system support. When a notification mechanism is used, a device can be safely powered down by software, and the port can then be powered off, allowing removal and insertion of a new device while the system is still on.



Integrating this controller into the ICH6 enhances the longevity of the platform. Serial ATA supports usage models such as digital video production, digital audio storage and recording, high-speed file sharing, and other data intensive applications.

## 2.5 SATA with the Advanced Host Controller Interface (AHCI)

AHCI is an industry-defined specification for Serial ATA host controller registers and command operations. The AHCI contained in the ICH6R offers features for improved drive performance and flexibility. This controller enables all SATA devices connected to any of the four SATA ports to function independently as 'masters' thereby eliminating the need for a master/slave designation.

The Native Command Queuing (NCQ) feature, when combined with an equivalently capable drive, allows commands to be transacted from system memory. After commands are sent to the SATA drive, they are executed in an optimized order minimizing mechanical positioning (both seek and rotational) latencies on the drive thereby providing faster transactions. ICH6 with AHCI enables software to efficiently issue up to 32 commands to a drive while automatically processing requests from the drive to transfer data without software intervention. Additionally, AHCI is capable of reporting multiple command completions simultaneously, enabling additional software overhead/interrupt reduction.

ICH6R AHCI provides refined hot plug support via an interlock switch mechanism. When appropriately implemented, hardware comprehends when a hot swap event has occurred without the need for prior software notification.

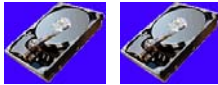
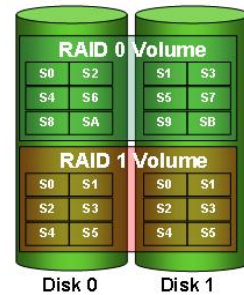
## 2.6 SATA with Intel® Matrix Storage Technology

By integrating the Intel Matrix Storage Technology controller into the I/O controller hub, there are neither PCI bandwidth limitations (133 MB /s) nor any loss of PCI resources (request/grant pair, PCI slot) that would typically occur with discrete PCI RAID solutions. The ICH6R includes an integrated RAID controller that uses the Serial ATA ports allowing for a variety of different RAID array options:

- RAID Level 0: ‘Data striping’ allows for a high-performance configuration with a maximum theoretical transfer rate of 300 MB/s. This configuration is used for increased performance with applications, playing games, video editing, etc.
- RAID Level 1: ‘Data mirroring’ provides data redundancy for information reliability. This configuration can be used to store critical data such as pictures and movies, personal data files, or any other valuable information that should not get lost.

- Two Volumes per SATA RAID Array: Creates a RAID 1 volume spanning a partition of the array while using the remainder of the array to create a RAID 0 volume. This flexible configuration allows for both increased performance and critical data storage.

Two Volumes per SATA RAID Array



RAID Level 0 and RAID Level 1 support is enabled by combining two Serial ATA hard drives on any two of the four SATA ports of the ICH6R. Additionally, a third SATA drive can be used as a ‘spare’. In the event of a drive failure in a RAID Level 1 configuration, with auto rebuild enabled and a designated spare attached, the spare and the good drive from the original array are used to recreate the RAID array.

Intel Matrix Storage Technology on ICH6R requires the following components:

- 2 Serial ATA hard disk drives
- Optional 3<sup>rd</sup> Serial ATA drive as a ‘spare’ for RAID Level 1 array rebuild capability
- Intel® Application Accelerator RAID Edition software
- System BIOS that includes the Intel Matrix Storage Technology Option ROM

§

## 3 Additional Features

---

The ICH6 includes a variety of other capabilities to improve the platform performance, reduce costs, and add functionality. Some of those features are described here:

### 3.1 High-Speed USB 2.0

The ICH6 provides eight high-speed USB 2.0 ports, providing 40 times the bandwidth of full-speed USB. Each of the ICH6's USB ports support high-speed, full-speed, and low-speed USB devices. To achieve this capability on all eight ports,

the ICH6 includes an Enhanced Host Controller Interface (EHCI) controller and four Universal Host Controller Interface (UHCI) controllers. The EHCI controller supports high-speed USB signaling for data transfers up to 480 Mb/s on all eight ports. Each of the UHCI controllers supports full-speed and low-speed USB signaling on two of the ports. When a device is plugged in, the ICH6's port routing logic will differentiate whether a high-speed USB device or a classic USB device is connected, and configures the appropriate UHCI or EHCI to take command of the device.



### 3.2 Alert Standard Format (ASF) Management Controller

The ASF controller, in conjunction with the integrated LAN controller, enables interface system-monitoring devices to communicate through the integrated LAN controller to the network. This means remote manageability and system hardware monitoring are made possible using ASF.

The ASF controller can collect and send various types of information from system components such as the processor, chipset, BIOS and sensors on the motherboard to a remote server running a management console. The controller can also be programmed to accept commands back from the management console and execute those commands on the local system.

Some examples of ASF alerting capabilities include monitoring system health information, such as BIOS messages, POST alerts, OS failure notifications, and system heartbeat signals to indicate the system is accessible to the server. Also included are system environmental notifications such as thermal, voltage and fan alerts, which the ASF controller can send as proactive warnings that something is wrong with the hardware. ASF can also monitor physical tampering by providing messages such as "cover tampered" to notify of potential system break-ins and processor or memory theft. Remote-control capabilities allow remote power-up, power down, power cycle, reset or reboot. If necessary, the system can be commanded to reboot to multiple boot paths. The system can also be pinged to ensure that it is on the network and running correctly.



### 3.3 AC '97 2.3 Controller

The ICH6 integrates an *Audio CODEC '97 Component Specification, Version 2.3* controller that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC) or a combination of ACs and a single MC (concurrent use of AC '97 and Intel High Definition Audio is not supported). The ICH6 supports up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Subwoofer, for a fulfilling surround-sound experience. ICH6 has expanded support for up to three audio codecs on the AC-link.

In addition, an AC '97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The ICH6-integrated AC '97 controller allows up to three external codecs to be connected to the ICH6. The system designer can provide AC '97 modem with a modem codec, or both audio and modem with up to two audio codecs with a modem codec.

### 3.4 LAN Controller

In conjunction with the Intel® 82562 family of products, the ICH6's integrated LAN provides a 32-bit PCI device and a 10/100 Ethernet controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS).

### 3.5 PCI Interface

The ICH6 provides a 33 MHz, 32-bit, PCI 2.3 implementation. The ICH6 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH6 requests. This allows for combinations of up to six PCI down devices and PCI slots.

### 3.6 System Management Bus (SMBus 2.0)

ICH6 provides an SMBus 2.0 Host Controller for the CPU to initiate communications with SMBus peripherals. In addition, ICH6 is also capable of operating in a mode in which it can communicate with I<sup>2</sup>C compatible devices. The ICH6 SMBus includes a slave interface which allows an external master to write or read to the ICH6 using the Host Notify Protocol. ICH6's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

### 3.7 IDE Interface

The fast IDE interface supports up to two IDE devices on a single channel providing an interface for IDE hard disks and ATAPI devices. The IDE interface supports Ultra ATA transfers up to 100 MB/s. The ICH6's IDE system contains a single IDE channel that can be configured to the standard primary or secondary channel (two devices).

§





## ***Appendix A***

---

For additional details and specifications, contact your local Intel Field Representative.

§